IN THE SPECIFICATION:

Please amend paragraph number **[0003]** as follows:

[0003] State of the Art: An integrated circuit (IC) typically includes a semiconductor die (die) electrically attached to a lead frame providing physical support for the die and connecting the die to external circuitry, such as a printed circuit board or other ~~conductor-carrying~~ conductor-carrying substrate. In such an arrangement, the lead frame and die may be connected by wire bonding the lead fingers of the lead frame to contact or bond pads located on a surface of the die. The die and lead frame are then typically encapsulated within a transfer-molded plastic package, although ceramic and metal packages may also be used, depending on the operating environment and the packaging requirements of the die.

Please amend paragraph number **[0004]** as follows:

[0004] As the demand for memory, in particular random access memory (RAM), surpassed the memory capability of a single die, ~~multichip~~ multi-chip modules (MCMs) were developed, such modules having a number of memory devices attached to a single substrate, such as a printed circuit board. A SIMM is a memory module having multiples of the same basic die, where the semiconductor memory chips are aligned in a row and interconnected to a printed circuit board to, in effect, create a single device with the memory capacity of the combined memory chips. An example of a ~~SIMM~~ SIMM, including a plurality of dynamic random access memory devices (DRAMs) used as memory in a ~~computer~~ computer, is illustrated in United States Patent 4,992,850, issued February 12, 1991, to Corbett et al., assigned to the assignee of the present invention. As the demand for additional memory on a single device has increased, other ~~devices~~ devices, such as dual in-line memory modules ~~(DIMMs)~~ (DIMMs), have also been developed. Such devices, while providing the desired memory capability on a single printed circuit board, present unique problems for the manufacturer when one or more of the semiconductor memory chips thereon fail.

Please amend paragraph number **[0005]** as follows:

[0005] It is well known that semiconductor dice have an early failure rate, often referred to in reliability terms as "infant mortality." Moreover, infant mortality of MCMs is multiplied depending on the number of individual semiconductor dice provided therein. For example, a SIMM composed of ten dice, each die having an individual reliability yield of 95%, would result in a first pass test yield of less than 60%, while ~~an SIMM~~ a SIMM composed of twenty dice, each die having an individual reliability yield of 95%, would produce a first pass test yield of less than 36%.

Please amend paragraph number **[0006]** as follows:

[0006] When a single packaged die, such as a dual in-line package (DIP), fails, a manufacturer can attempt to repair the device, use the device for some reduced capacity function if the device is only partially defective, or scrap it. When complete failure of a die has not occurred and a portion of the memory is good (e.g., 1, 2, or 3 megabits of ~~a 4 megabit~~ a 4-megabit chip), such a device is not typically useful. For MCMs such as a SIMM, where a number of semiconductor dice are attached to a single substrate, however, it may not be possible to use the device for some reduced capacity function and it is surely not desirable to scrap the entire MCM when some, if not most, of the dice attached thereto are not defective. Thus, the manufacturer is left with the somewhat costly process of reworking the MCM, typically by removing the defective chips and replacing them with new ones. Such a procedure is described in United States Patents 5,239,747 and 5,461,544, where a SIMM having a specialized trace pattern suitable for both burn-in and individual die testing is tested to determine if any of the semiconductor devices mounted thereon are non-functional and, if so, either the defective device is replaced with a device which has been subjected to burn-in, or the entire ~~multichip~~ multi-chip module can be subjected to another burn-in process after the replacement of the defective device. The defective devices, however, are merely replaced by removing the defective device and replacing it with another device either previously subjected to burn-in or not. This rework process can be complicated, time consuming and costly, depending upon the type of device, the

type of mounting of the device on the substrate, and the type of substrate used for mounting. For example, plastic-packaged devices are typically physically pulled to disconnect their leads from the module, while so-called "glob topped" (silicone or epoxy gel covering) dice may be removed after cutting through the encapsulant to the wire-bonded die, which is pulled. In addition, since replacing multiple unacceptable dice on ~~an MCM~~ a MCM poses physical risks to other MCM dice during the replacement operation, it may be desirable to discard such ~~an MCM~~ a MCM rather than attempt rework, particularly where the reliability of the replacement die is not known.

Please amend paragraph number **[0008]** as follows:

[0008] A cost-effective method for producing known reliable SIMMs, DIMMs, and the like, with larger numbers of chips on a single device is desirable for industry acceptance and use. In an attempt to provide known reliable SIMMs complying with consumer requirements, it would be desirable to fabricate the SIMM completely of KGD. Using only KGD in a SIMM, however, would not currently be cost effective since each KGD has to be subjected to performance and burn-in testing, both of which are costly at this point in time. Typically, however, SIMMs are fabricated from probe-tested dice, and are subsequently burned-in and performance tested. In contrast to the use of all KGD in a SIMM, when using dice with well known production and reliability histories, particularly where the dice being used are known to have a low infant mortality rate, the use of such minimally tested dice to produce ~~an SIMM~~ a SIMM is usually found to be the most cost effective alternative.

Please amend paragraph number **[0009]** as follows:

[0009] As previously stated, since typical testing and burn-in procedures are generally labor and time intensive, posing significant risks to the dice of a SIMM, in the event that a SIMM contains an unacceptable die, replacement of the unacceptable die with a KGD is preferable. Module rework with a KGD does not typically require the SIMM to be subjected to additional burn-in procedures that can unnecessarily stress the dice. An example of a method and apparatus for the testing and burn-in of an individual die prior to packaging is illustrated in United States

Patent 5,424,652, issued June 13, 1995, to Hembree et al., assigned to the assignee of the present invention. Such a method and apparatus provide a source of KGD to allow for the rework of an unacceptable die in ~~an MCM~~ a MCM with a KGD. In other instances, it is known to test a die in a package for functionality and replace any defective die. Such is illustrated in United States Patents 5,137,836, 5,378,981, and 5,468,655.

Please amend paragraph number **[0010]** as follows:

[0010] One way in the art to eliminate the need to physically remove defective or unacceptable dice from a SIMM has been to provide additional, redundant spaces on the printed circuit board for attachment of replacement chips. Thus, one additional space has been provided adjacent each memory chip on the board, the additional spaces providing contacts for attachment of a semiconductor chip similar to the one it is replacing. For example, if a ~~32 megabit~~ 32-megabit SIMM contains eight ~~4 megabit~~ 4-megabit chips, then eight additional spaces are provided on the SIMM, configured to accept up to eight additional ~~4 megabit~~ 4-megabit chips, if necessary. Such a configuration, however, results in a memory module that is approximately twice as big as a memory module having no extra spaces.

Please amend paragraph number **[0013]** as follows:

[0013] In a preferred embodiment, a SIMM or DIMM board is provided having a plurality of primary chip attach locations and one auxiliary chip attach location. Each of the plurality of primary chip attach locations is similarly configured to accept the same type of semiconductor chip, such as a number of ~~4 megabit~~ 4-megabit chips. The auxiliary chip attach location, on the other hand, is configured to accept more than one capacity of replacement semiconductor chip. Thus, depending on the amount of defective memory detected on the SIMM, a replacement chip having at least that amount of good memory can be attached to the auxiliary chip attach location. Consequently, the replacement chip may be a ~~1 megabit~~ 1-megabit chip, if only ~~one 1~~ one (1) megabit of memory is found defective, or a ~~4 megabit~~

4-megabit chip, if an entire ~~4 megabit~~ 4-megabit chip is found to be defective, the configuration of the auxiliary chip attach location being capable of accepting either replacement chip.

Please amend paragraph number **[0015]** as follows:

[0015] Having the capability to easily and cost effectively rework memory modules without the need to remove defective chips or the need to substitute defective chips on a ~~one-to-one~~ one-to-one basis is highly desirable. The ability to provide auxiliary chip attach locations that can accommodate a plurality of different chip configurations not only makes rework more simple, but allows memory modules with large numbers of chips to be cost effective. For example, in yet another preferred embodiment, a memory module having three rows of similar memory chips is provided with more than one auxiliary chip attach location, each of the auxiliary chip attach locations being capable of receiving more than one type of semiconductor die. Thus, if only one of the many chips provided thereon fails entirely, then one substantially identically configured chip can be attached to any one of the three auxiliary chip attach locations. If more than one memory chip fails or more defective memory is located than can be replaced with a single auxiliary chip, then, if necessary, more than one replacement chip can be attached to any one or more of the three auxiliary chip attach locations.

Please amend paragraph number **[0016]** as follows:

[0016] In yet another preferred embodiment, rather than having all of the auxiliary chip attach locations capable of receiving variously configured chips, at least two auxiliary chip attach locations are each provided with different configurations. Thus, depending on the number of bad memory chips, one or more chips having a combined memory capacity substantially equal to the bad memory can be attached to the auxiliary chip attach locations. For example, on a DIMM with five ~~4 megabit~~ defective 4-megabit chips ~~found defective,~~ found, a replacement ~~16 megabit~~ 16-megabit chip can be attached to the auxiliary chip attach location configured to receive ~~16 megabit~~ 16-megabit chips and a replacement ~~4 megabit~~ 4-megabit chip can be attached to the auxiliary chip attach location configured to receive a ~~4 megabit~~ 4-megabit chip.

Please amend paragraph number **[0017]** as follows:

[0017] Preferably, the replacement chips are KGD so that the additional burn-in is not required on the memory module. Moreover, the KGD may be partially defective dice or "partials" that are known to be good for a certain capacity of memory (e.g., 3 megabits of ~~a 4 megabit~~ a 4-megabit chip). This is particularly attractive, since a high percentage (approaching 50%) for some designs of ~~16 megabit~~ 16-megabit DRAMS is partially or completely defective, while 5-10% of ~~4 megabit~~ 4-megabit DRAMS comprise partials. Since partials might otherwise be discarded, beneficial use thereof as replacement chips enhances the effective yield rate for the chips and lowers ~~per unit memory~~ per-unit memory costs.

Please amend paragraph number **[0018]** as follows:

[0018] Thus, for example, for a SIMM having a design memory capacity of 32 megabits with 7 of the 32 megabits tested defective, a replacement partial ~~16 megabit~~ 16-megabit chip known to be good for 7 megabits could be attached to an auxiliary location. The defective memory of 7 megabits on the primary chip(s) could then be disabled. Similarly, for a ~~32 megabit~~ 32-megabit memory module with 7 bad megabits of memory and more than one auxiliary chip attach location, a replacement full ~~4 megabit~~ 4-megabit KGD and a ~~3 megabit~~ 3-megabit "partial" KGD could be attached to two of the auxiliary chip attach locations.

Please amend paragraph number **[0033]** as follows:

[0033] Accordingly, if during intelligent burn-in of the SIMM 10 one of the ten chips 14 shown in FIG. 1 completely fails, then a replacement chip of substantially similar configuration to chips 14 can be attached to the inner array 28 to replace the failed chip 14. As illustrated in FIG. 3, however, if more than one chip 14 fails or memory equaling the capacity of more than one chip is proven defective during burn-in, it may be necessary to connect a ~~larger capacity~~ larger-capacity replacement chip 50 to the auxiliary chip attach location, one that provides enough memory to replace the combined memory of the failed chips 14.

Please amend paragraph number **[0034]** as follows:

[0034] It should be noted that the replacement chip may be attached to the module by a technique different from that used to connect chips 14. Thus, the replacement chip may be ~~wire-bonded~~ wire-bonded for ease of attachment, while the chips 14 were flip-chip attached by solder reflow. The replacement chip may then be separately glob-topped or otherwise protected after wire bonding, the primary chips having been previously underfilled and encapsulated during initial fabrication of the module.

Please amend paragraph number **[0037]** as follows:

[0037] Similarly, in FIG. 6, a memory module 90 having thirty individual memory chips 92 is made possible by providing at least one auxiliary chip attach location 94. Because of the difficulty associated with reworking a device having so many potentially defective chips, manufacturing such a device as memory module 90 would typically not even be attempted without the exclusive use of pretested known-good-die (KGD). The exclusive use of KGD primary chips would clearly not be cost-~~effect~~ effective because of the cost associated with testing each chip individually before attaching it to the memory device.

Please amend paragraph number **[0038]** as follows:

[0038] As illustrated in FIG. 6, it may be desirable to provide more than one auxiliary chip attach location 94 such as auxiliary locations 96 and 98. Such a configuration has added benefits because it provides more flexibility for the type and number of chips that can be attached thereto. For example, if four of the memory chips 92 are found completely defective, each of the chips 92 having a design memory capacity of 16 megabits, and another chip 92 exhibits 3 ~~megabytes~~ megabits of defective memory, then a ~~3 megabit (partial 4 megabit)~~ 3-megabit (partial 4-megabit) chip 100 can be attached to auxiliary location 98 and a ~~64 megabyte~~ 64-megabit chip 102 attached to auxiliary location 96. Various other combinations could also be devised depending on the KGD on hand and the memory size of those KGD.

Please amend paragraph number **[0041]** as follows:

[0041] Finally, as shown in FIG. 9, the multi-chip modules of the various preferred embodiments herein described, such as SIMM 10 of FIG. 1, can be incorporated into a memory device 130 of an electronic system 132, such as a computer system, that includes an input device 134 and an output device 136 coupled to a processor device 138. Of course, the ~~multi-chip~~ multi-chip module 10 can alternatively be incorporated into the input device 134, the output device 136, or the processor device 138.

Please amend paragraph number **[0042]** as follows:

[0042] It will be appreciated by those skilled in the art that various methods can be used to achieve the desired memory capability of the memory device, such as use of enabling and/or disabling devices 118 located on each chip 116 of FIG. 7. The enabling and/or disabling devices 118 may include fuses, antifuses, and other such devices known in the art that can fully or partially disable the memory capacity of a chip 116. Furthermore, a programmable ~~device~~ device, such as a so-called "traffic control" ~~EEPROM~~ EEPROM, as known in the ~~art~~ art, may be installed on each module and programmed based on burn-in results to reroute input and output paths and link the new KGD auxiliary chips to the remainder of memory on the module so as to present an interface to the mother board or other higher-level ~~packaging~~ packaging, which is indistinguishable to the host system from a perfect as-fabricated module with 100% good primary or original memory. Such a traffic control EEPROM is illustrated at 86 in FIG. 5.

Please amend paragraph number **[0044]** as follows:

[0044] It should be noted that the term ~~"chip",~~ "chip," as used in the specification and appended claims, is intended as exemplary and not limiting, the invention having applicability to any packaged die, bare die, and/or any intermediate product thereof. In addition, while the preferred embodiments were illustrated as being flip-chip bonded to the substrate, the dice, whether replacement or otherwise, may be wire bonded or otherwise electrically attached to the substrate as known in the art.